SGS-THOMSON MICROELECTRONICS

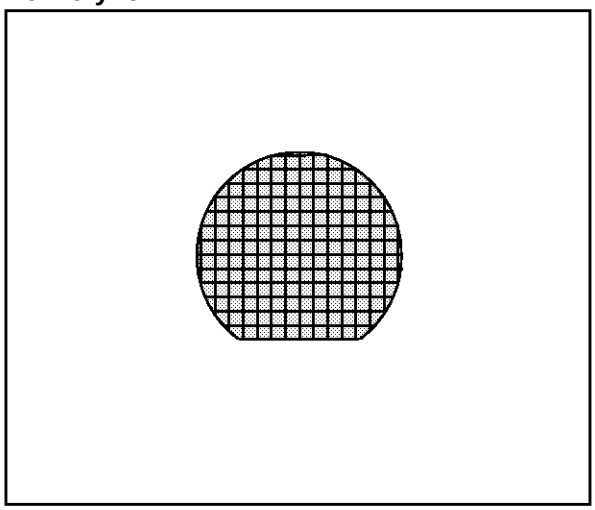
ST16SF48

CMOS MCU BASED SAFEGUARDED SMART CARD IC WITH 8176 bytes EEPROM

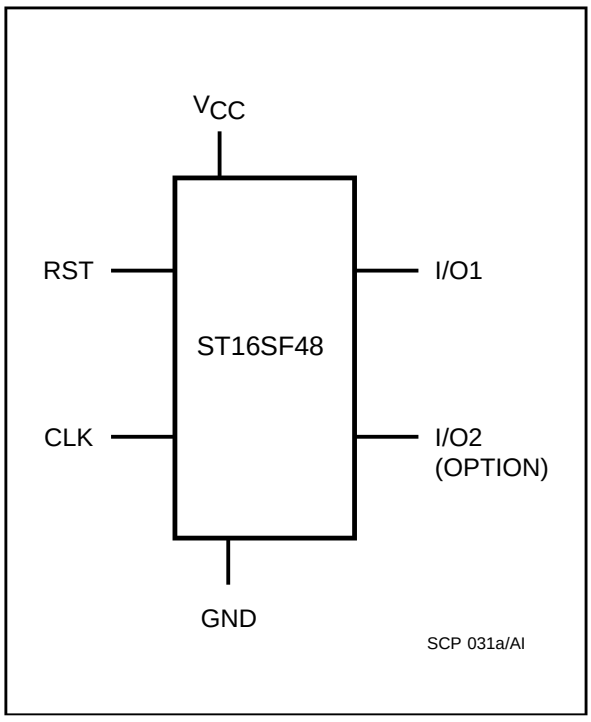
BRIEF DATA

- EXTENDED VOLTAGE OPERATION
  - Vcc Range : 2.7V to 5.5V
- 8 BIT ARCHITECTURE CPU
- 16 Kbytes OF USER ROM, SECTOR COMBINATIVE
- 1.5 Kbytes OF SYSTEM ROM.
- 384 bytes OF RAM
- 8176 bytes OF EEPROM, SECTOR COMBINATIVE
  - Highly reliable CMOS EEPROM technology
  - 10 years data retention
  - 100 000 Erase/Write cycles endurance
  - Protected One Time Programmable block (32 or 64 bytes)
  - 1 to 32 bytes block Erase or Write in single cycle programming
- SERIAL ACCESS, ISO 7816-3 COMPATIBLE
- STANDBY MODE FOR POWER SAVING
- UP TO 5 MHz INTERNAL OPERATING FREQUENCY
- VERY HIGH SECURITY FEATURES INCLUDING EEPROM FLASH ERASE
- CONTACT ASSIGNMENT COMPATIBLE ISO 7816-2
- ESD PROTECTION GREATER THAN 5000V
- 2 OPERATING CONFIGURATIONS
  - ISSUER
  - USER
- MEETS GSM 11.11 AND 11.12 SPECIFICATIONS

Delivery form



Pin Connection



Contact name

CLK	Clock
RST	Reset
I/O1	Data Input/Output
I/O2	Data Input / Output (option)
Vcc	Supply Voltage
GND	Ground

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INTRODUCTION

The ST16SF48, a member of the standard ST16xyz family of devices, is a serial access microcontroller especially designed for very large volume smart cards applications requiring a large amount of data, where firmware security algorithm must be implemented. The ST16SF48 is based on 8 bit CPU core and includes on chip memories : 384 bytes of RAM, 16 Kbytes of USER ROM, 1.5 Kbytes of SYSTEM ROM, and 8176 bytes of EEPROM.

Both ROM and EEPROM memories can be configured into two sectors. Access rules from any memory section or sector to any other are set-up by User's defined Memory Access Control Matrix (MACM).

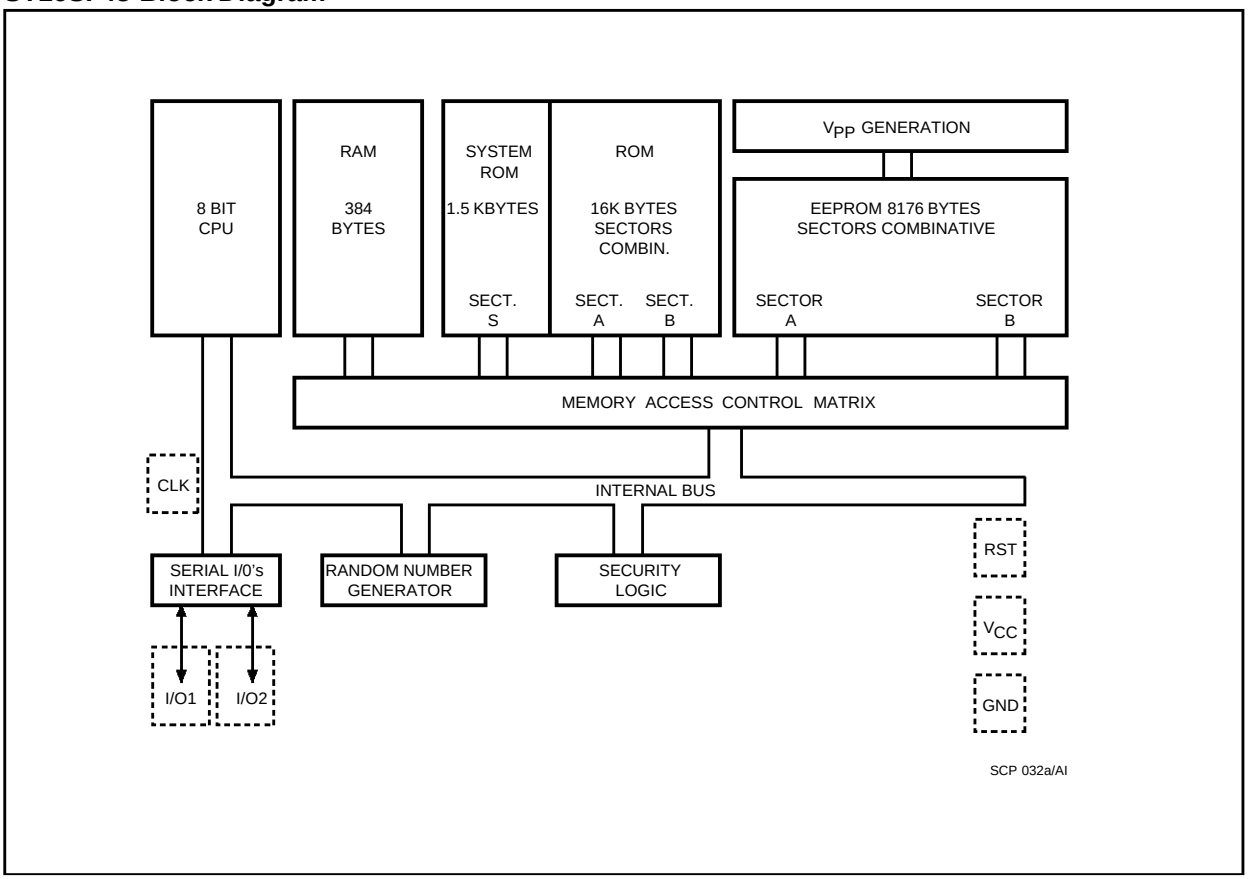
Reliability data related to the ST16SF48 product manufactured using SGS-THOMSON 1µ CMOS EEPROM technology confirm data retention up to 10 years and endurance up to 100,000 Erase/ Write cycles.

As all the other ST16xyz family members, the ST16SF48 is fully compatible with the ISO standards for smart cards applications.

Software development (ROM code, options) can be done with the ST16S-EMU development system.

The ST16SF48 can be delivered either in unsawn or sawn wafers, 180 or 275 micron thickness.

ST16SF48 Block Diagram



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ST16SF48 STANDARD MANAGER

The ST16SF48 Manager is an executable code in accordance to the SGS-THOMSON Chip Manager concept, implemented on the ST16SF48 MCU based Smartcard IC.

It allows easy access to ST16SF48 memories through an extensive set of commands.

The ST16SF48 Manager is designed to reduce the time required for the fabrication of any ROM-masked product and to offer the user direct entry to the application, as well as giving easy access to the ST16SF48 product for evaluation.

A patch is a code that can be loaded in EEPROM, in order to modify the Manager behaviour.

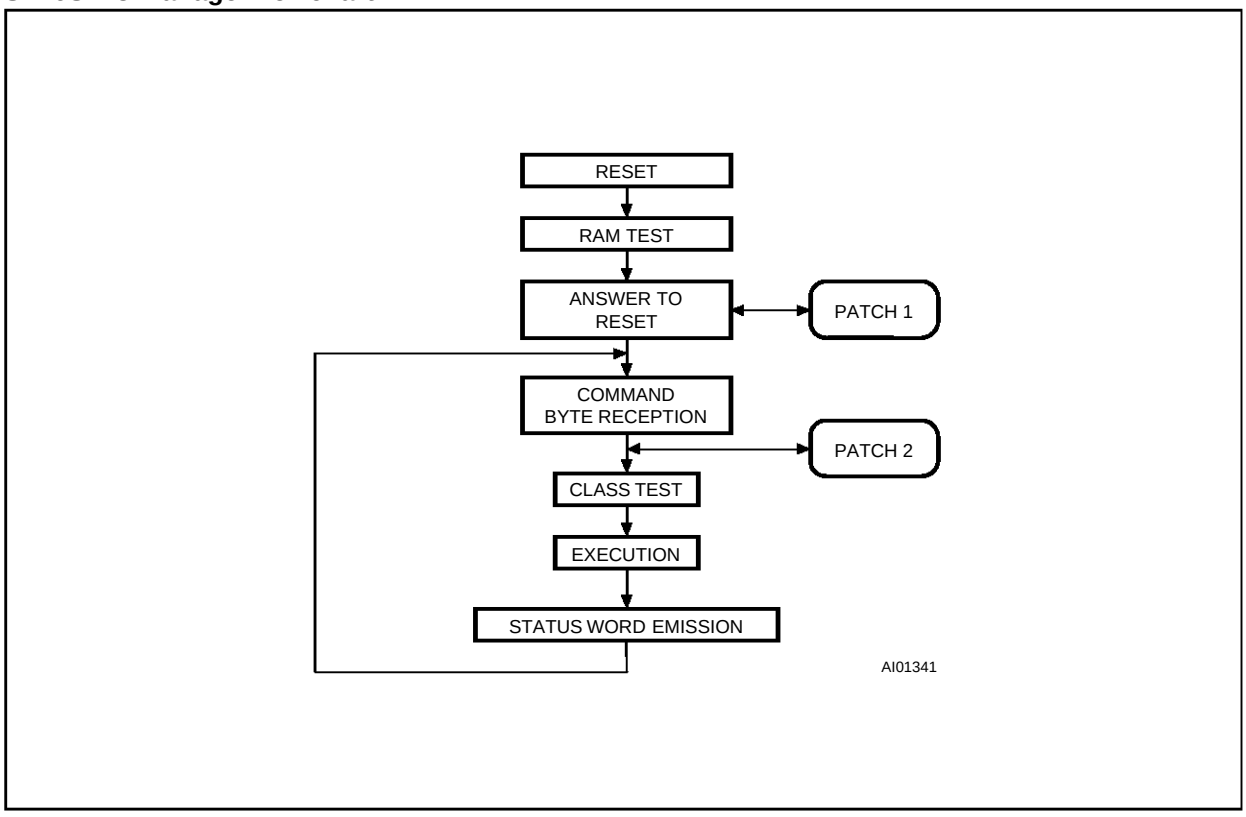
Patch 1 allows Answer To Reset modification and patch 2 allows received command modifications.

MANAGER FEATURES

In addition to the standard commands, using the ISO 7816-3 standard protocol, the user may set/reset the following features of the ST16SF48 Manager:

- ISO protocol selection inverted or direct convention.
- Output selection: I/O1 or I/O2.
- I/O input: polling or interrupt from stand-by.
- I/O baud rate selection, allowing high baud rate with slow clocks.
- CLK frequency selection, allowing high baud rate with slow clocks.
- Security register management.
- EEPROM programming delay.
- Patches: conditional extension branch.

ST16SF48 Manager flowchart



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